Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 76 are presently pending in the application. Claims 1 - 38 are subject to examination and claims 39 - 76 have been withdrawn from examination. Claims 1, 3, 20 and 22 have been amended. Claims 77 - 78 were previously canceled. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In item 3 of the above-identified Office Action, claims 1, 3, 20 and 22 were rejected as allegedly being indefinite under 35 U.S.C. § 112, second paragraph. More specifically, it was alleged in the Office Action that claims 1 and 20 were indefinite for using the phrase "like a configuration" and claims 3 and 22 were indefinite for using the phrase "potential data signals". Applicant has amended claims 1, 3, 20 and 22 to address the concerns raised in item 3 of the Office Action. For example, claims 3 and 22 were amended to delete the word "potential". Further, claims 1 and 20 were amended to recite that, among other limitations, the structurable hardware unit is configured "**in the same ways that**" field-programmable logic arrangements including PLAs, GLAs, PLDs, or FPGAs are configured.

The amendments to claims 1 and 20 are supported by the specification of the instant application, for example, page Support for these changes may be found on page 25 of the instant application, lines 4 - 13, which state:

> **The configuration of the configurable elements of the SLE layer**, i.e. the configuration of the multiplexers, the configurable connections within the structurable logic arrangements and the registers **can essentially be effected like the configuration of the known field-programmable logic arrangements (PLAs, GALs, PLDs, FPGAs etc.)**.
>
> A first possibility **in this respect consists in the (irreversible) production or erasure of connections using so-called fuses or antifuses.** [emphasis added by Applicant]

See also, page 25 of the instant application, line 5 - page 26, line 9, for other disclosed configurations.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, second paragraph.

In item 5 of the Office Action, claims 1 - 7, 10 - 11, 13 - 26, 29 - 30 and 32 - 38, were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,598,148 to Moore et al ("**MOORE**") in view of U. S. Patent No. 6,279,045 to Muthujumaraswathy et al ("**MUTHUJUMARASWATHY**"). In item 22 of the Office Action, claims 8, 9, 12, 27, 28 and

31, were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **MOORE** in view of **MUTHUJUMARASWATHY**, and further in view of United States Patent No. 5,825,878 to Takahashi et al ("**TAKAHASHI**").

Applicant respectfully traverses the above rejections.

More particularly, Applicant has amended claim 1 to recite, among other limitations:

> **an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said plurality of units**, including at least one of an interface connection between said intelligent core and said internal peripheral units, an interface connection between said intelligent core and said external peripheral units, an interface connection between said intelligent core and said memory devices, and an interface connection between said plurality of units; [emphasis added by Applicant]

Applicant's independent claim 20 recites a similar limitation, among others. As such, Applicant's claims 1 and 20 require, among other limitations, **an application specifically configurable intelligent interface connecting the intelligent core to the plurality of units**. This limitation is supported by the specification of the instant application, for example, on page 10 of the instant application, lines 9 - 12, which state:

> The microcontroller considered herein is designated by the reference symbol 1 in the figures. **It is**

> **distinguished by the fact that it comprises one or more application-specifically configurable intelligent interfaces**. [emphasis added by Applicant]

Additionally, Applicant's amended claim 1 recites, among other limitations:

> **said application-specifically configurable intelligent interface including a structurable hardware unit including at least one of structurable data paths and structurable logic elements;** [emphasis added by Applicant]

Applicant's independent claim 20 was amended to recite a similar limitation, among others. As such, Applicant's claims 1 and 20 require, among other limitations, that the **application-specifically configurable intelligent interface connecting the intelligent core to the plurality of units includes a structurable hardware unit including at least one of structurable data paths and structurable logic elements**. The further amendments to claims 1 and 20, described above, are supported by the specification of the instant application, for example, page 11 of the instant application, lines 9 - 21, which state:

> **The SLE layer 12 is arranged in circuit terms between the µP core 11, peripheral units (for example the peripheral units 13 to 19) provided inside and/or outside the program-controlled unit, and/or memory devices (for example the RAM 2 and/or the ROM 3). It contains structurable data paths and/or logic elements which can be structured or configured in such a way that the SLE layer 12 can be used as the at least one application-specifically configurable interface**, more precisely as a configurable intelligent interface between the µP core

> and one or more peripheral units and/or between the µP core and one or more memory devices and/or between two or more peripheral units themselves and/or between one or more peripheral units and one or more memory devices. [emphasis added by Applicant]

Further, Applicant's amended claim 1 recites, among other limitations:

> **said structurable hardware unit being configured in the same ways that field-programmable logic arrangements including PLAs, GLAs, PLDs, or FPGAs are configured**, and to evaluate and process data and/or signals received.

Applicant's claim 20 was amended to recite a similar limitation, among others. As such, Applicant's claims 1 and 20 require, among other limitations, that the **application-specifically configurable intelligent interface connecting the intelligent core to the plurality of units includes a structurable hardware unit including at least one of structurable data paths and structurable logic elements, configured in the same ways that field-programmable logic arrangements are configured**. The above limitation is supported by the specification of the instant application, for example, on page 25 of the instant application, line 4 - page 26, line 2, which state:

> **The configuration of the configurable elements of the SLE layer**, i.e. the configuration of the multiplexers, the configurable connections within the structurable logic arrangements and the registers **can essentially be effected like the configuration of the known field-**

> **programmable logic arrangements (PLAs, GALs, PLDs, FPGAs etc.).**
>
> **A first possibility in this respect consists in the (irreversible) production or erasure of connections** using so-called fuses or antifuses.
>
> **Another possibility consists in carrying out reversible configuration** based on data representing the desired configuration, the data being stored in EPROMS, EEPROMS or the like provided inside or outside the program-controlled unit. As a result, the configuration of the program-controlled unit can be changed a limited number of times.
>
> **A further possibility consists in carrying out reversible configuration based on data representing the desired configuration,** but where the data are stored in a RAM or the like. As a result, the configuration of the program-controlled unit can be changed an unlimited number of times and very rapidly. [emphasis added by Applicant]

As such, Applicant's particularly claimed configurable interface of claims 1 and 20 can be configured using the same configuration/production methods used to configure of other field programmable logic devices.

The cited references, taken alone or in combination, fail to teach or suggest, among other limitations of Applicant's claims, **an application-specifically configurable intelligent interface connecting the intelligent core to the plurality of units and including a structurable hardware unit including at least one of structurable data paths and structurable logic elements, configured in the same ways that field-programmable logic arrangements are configured.**

More particularly, the **MOORE** reference discloses a high performance microprocessor having a variable speed system clock and including a processing unit designed to operate in accordance with a predefined sequence of program instructions stored within an instruction register. However, the **MOORE** reference fails to teach or suggest, among other limitations of Applicant's claims, **an application specifically configurable intelligent interface connecting the intelligent core to the plurality of units**, as particularly required by Applicant's claims 1 and 20.

Rather, the Office Action points to col. 14 of **MOORE**, line 62 - col. 15, line 20, as allegedly disclosing Applicant's previously claimed "application specifically configurable intelligent interface". Applicant respectfully disagrees.

Col. 14 of **MOORE**, line 62 - col. 15, line 20, states:

> ASYNCHRONOUS/SYNCHRONOUS CPU
>
> Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (FIG. 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display

> updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. **The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data.** The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. **By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface** 432, optimum performance can be achieved by each. **Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals** on lines 436, with data/addresses passing on bus 90, 136.

However, the interface 432 of **MOORE** is not **an application specifically configurable intelligent interface connecting the intelligent core to the plurality of units**, as particularly required by Applicant's claims 1 and 20. The decoupling and recoupling of the CPU from the fixed speed of the I/O interface 432 of **MOORE** neither teaches, nor suggests, among other limitations of Applicant's claims, an **application-specifically configurable intelligent interface connecting the intelligent core to the plurality of units and including a structurable hardware unit including at least one of structurable data paths and structurable logic elements**, as presently required by Applicant's claims 1 and 20. First, the decoupling/recoupling of the clock speed of the CPU to the Interface 432, disclosed in **MOORE**, fails to teach or suggest, among other limitations of Applicant's claims 1 and 20, that the **interface is application specifically configurable**. Further, the decoupling/recoupling disclosed in **MOORE** fails to

teach or suggest, among other limitations of Applicant's claims 1 and 20, that the **interface** is **configurable because it includes a structurable hardware unit including at least one of structurable data paths and structurable logic elements**, as currently recited in Applicant's amended claims 1 and 20.

Further still, as acknowledged on page 4 of the Office Action, **MOORE** fails to teach or suggest, among other limitations of Applicant's claims 1 and 20, that the hardware unit is configured "like a configuration of field programmable logic arrangements". As discussed above, Applicant's claims 1 and 20 have been amended to recite, among other limitations, that the configurable hardware unit of the interface, and thus the interface, is **configured in the same way that other field programmable logic arrangements are configured**. The **MOORE** reference additionally fails to teach or suggest, among other limitations of Applicant's claims, **an interface connected between the intelligent core and a plurality of units, which interface is application specifically configured in the same way that other field programmable logic arrangements are configured**, as currently required by Applicant's claims 1 and 20.

In view of the foregoing, it can be seen that Applicant's claims 1 and 20 are patentable over the **MOORE** reference.

However, even the combination of **MOORE** and **MUTHUJUMARASWATHY**, as cited in the Office Action, does not teach or suggest all limitations of Applicant's invention of claims 1 and 20. Like **MOORE**, **MUTHUJUMARASWATHY** fails to teach or suggest, among other limitations of Applicant's claims, **an application-specifically configurable intelligent interface connecting the intelligent core to the plurality of units and including a structurable hardware unit including at least one of structurable data paths and structurable logic elements, configured in the same ways that field-programmable logic arrangements are configured**. Like **MOORE**, **MUTHUJUMARASWATHY** fails to teach or suggest, among other limitations of Applicant's claims, an **application-specifically configurable** intelligent **interface** connecting an intelligent core to a plurality of units. Further, **MUTHUJUMARASWATHY** fails to teach or suggest, among other limitations of Applicant's claims **an interface that includes at least one of structurable data paths and structurable logic elements, configured in the same ways that field-programmable logic arrangements are configured**.

Instead, **MUTHUJUMARASWATHY** discloses a multimedia interface having a multimedia processor and a field programmable gate array (FPGA). Although **MUTHUJUMARASWATHY** discloses that the invention, in its entirety, is directed towards a multimedia

interface, it does **not** teach or suggest, that the interface is application specifically configurable to connect an intelligent core to a plurality of units. Rather, in **MUTHUJUMARASWATHY**, the "interface" disclosed in the title and abstract is **the core, FPGA and the units**, and **not** an interface connected **between** a core and a plurality of units, as required by Applicant's claims 1 and 20. Further, the FPGA in **MUTHUJUMARASWATHY** is **not** an interface between an intelligent core and a plurality of units, as claimed by Applicant's claims 1 and 20.

In view of the foregoing, it can be seen that the **MOORE** and **MUTHUJUMARASWATHY** references, taken alone or in combination, fail to teach or suggest all limitations of Applicant's claims 1 and 20. For example, the combination of **MOORE** and **MUTHUJUMARASWATHY** still fails to teach or suggest, among other limitations of Applicant's claims, the **particularly** claimed application specifically configurable intelligent interface, of Applicant's amended claims 1 and 20. Thus, Applicant's claims 1 and 20 are believed to be patentable over the **MOORE** and **MUTHUJUMARASWATHY** references.

The **TAKAHASHI** reference, cited in the Office Action in combination with **MOORE** and **MUTHUJUMARASWATHY** against certain of Applicant's dependent claims, does not cure the above-

discussed deficiencies in the **MOORE** and **MUTHUJUMARASWATHY** references.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 20. Claims 1 and 20 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 20.

In view of the foregoing, reconsideration and allowance of claims 1 - 76 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

The present Amendment is being filed simultaneously with a Request for Continued Examination (RCE) and the associated fee. Additionally, please consider the present as a petition for a one (1) month extension of time, and please provide a one (1) month extension of time, to and including, July 30, 2007, to respond to the present Office Action.

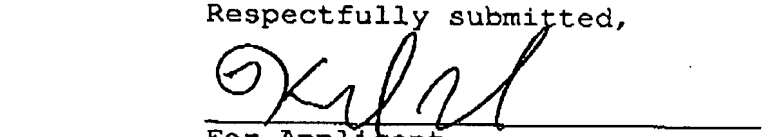
The extension fee for response within a period of one (1) month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please provide any additional extensions of time that may be necessary and charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



For Applicant

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July 30, 2007

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